Amendments to the Specification:

Please amend the first paragraph on page 7 as follows.

Fig. 1 shows a cross section view of an example of a floating gate pixel. An N well 12 is formed in a P type silicon substrate, usually a P type epitaxial silicon substrate. A P well 14 is formed in the N well 12. The only contact to the pixel structure is in the P well 14 and is shown as a single P^+ type contact 20 in Fig. 1. This P^+ type contact 20 allows the pixel to be reset and serves as a source/drain region. A gate oxide 18 is formed on the substrate and a gate electrode 16 is formed on the gate oxide 18. Although two sections of the gate electrode 16 are shown in Fig. 1 the two sections are part of a single gate electrode. The gate electrode has a closed shape such as a donut shape and is connected to an output terminal 22. The gate oxide 18 and the gate electrode 16 are directly over part of the P well 14, part of the N ~~well12~~ well 12, and the intersection of the PN junction 15 between the P well 14 and the N well 12 and the top surface 11 of the pixel. Alternatively the gate oxide 18 can cover the entire top surface 11 of the pixel, although this option is not shown in Fig. 1. An output amplifier 34, connected to the output terminal 22, is used to read the potential of the floating gate 16.